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2	15	(716/21.cccls. and ((offset or shift or move or shrink) same (line or segment))) and ((delet\$4 or remov\$4 or eliminat\$4) with (vertex orverticies or interconnect\$5 or locus or cluster or point))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/11/01 11:38
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-	1	((opc or (optical with (process or proximity with correction)) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4))) and (((ocr or (optical with (process or proximity) with recognition)) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4))) and (line or segment))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 19:38
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	565	716/21.cccls. and ((offset or shift or move or shrink) same (line or segment))	USPAT; US_PGPUB; EPO; JPO; IBM_TDB USPAT; US_PGPUB; EPO; JPO; IBM_TDB	2004/10/29 20:40
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Results of Search "L2"

	Document ID	Issue Date	Title	Current OR	Current XRef
1	US 20040209176 A1	20041021	Model-based data conversion	430/5	430/322; 716/19; 716/21
2	US 20040161679 A1	20040819	Full sized scattering bar alt-PSM technique for IC manufacturing in sub-resolution era	430/5	716/19; 716/21
3	US 20020160278 A1	20021031	Method for designing photolithographic reticle layout, reticle, and photolithographic process	430/5	430/322; 716/19; 716/21
4	US 20020132174 A1	20020919	Self-aligned fabrication technique for tri-tone attenuated phase-shifting masks	430/5	430/311; 430/312; 430/313; 430/394; 716/21
5	US 20020015899 A1	20020207	Hybrid phase-shift mask	430/5	430/322; 716/19; 716/21
6	US 6792590 B1	20040914	Dissection of edges with projection points in a fabrication layout for correcting proximity effects	716/19	430/5; 716/21
7	US 6785879 B2	20040831	Model-based data conversion	716/21	430/5; 716/19; 716/7; 716/8
8	US 6711732 B1	20040323	Full sized scattering bar alt-PSM technique for IC manufacturing in sub-resolution era	716/19	716/21

	Document ID	Issue Date	Title	Current OR	Current XRef
9	US 6625801 B1	20030923	Dissection of printed edges from a fabrication layout for correcting proximity effects	716/19	716/21
10	US 6546543 B1	20030408	Method of displaying, inspecting and modifying pattern for exposure	716/21	
11	US 6543045 B2	20030401	Method for detecting and automatically eliminating phase conflicts on alternating phase masks	716/21	716/19; 716/20
12	US 6539521 B1	20030325	Dissection of corners in a fabrication layout for correcting proximity effects	716/4	716/19; 716/21
13	US 6493866 B1	20021210	Phase-shift lithography mapping and apparatus	716/21	430/396; 430/5; 716/19; 716/4
14	US 5124927 A	19920623	Latent-image control of lithography tools	700/121	250/491.1; 356/394; 356/401; 702/94; 716/21
15	US 4559603 A	19851217	Apparatus for inspecting a circuit pattern drawn on a photomask used in manufacturing large scale integrated circuits	716/5	250/491.1; 250/492.2; 257/E21.21 1; 356/237.5; 356/394; 716/21

Results of Search "L1"

	Document ID	Issue Date	Title	Current OR	Current XRef
1	US 20040191650 A1	20040930	Phase shift masking for complex patterns with proximity adjustments	430/5	716/19
2	US 20030126582 A1	20030703	Pattern correction method and manufacturing method of semiconductor device	716/21	700/121; 716/19
3	US 20030023939 A1	20030130	METHOD AND APPARATUS FOR ANALYZING A LAYOUT USING AN INSTANCE-BASED REPRESENTATION	716/3	716/19; 716/4; 716/5; 716/8
4	US 20020127479 A1	20020912	Phase shift masking for complex patterns with proximity adjustments	430/5	
5	US 20020026624 A1	20020228	Correction of layout pattern data during semiconductor patterning process	716/11	716/10; 716/4
6	US 6792590 B1	20040914	Dissection of edges with projection points in a fabrication layout for correcting proximity effects	716/19	430/5; 716/21
7	US 6777138 B2	20040817	Mask product made by selection of evaluation point locations based on proximity effects model amplitudes for correcting proximity effects in a fabricat layout	430/5	

	Document ID	Issue Date	Title	Current OR	Current XRef
8	US 6733929 B2	20040511	Phase shift masking for complex patterns with proximity adjustments	430/5	430/30; 716/19
9	US 6687885 B2	20040203	Correction of layout pattern data during semiconductor patterning process	716/5	716/11; 716/19
10	US 6625801 B1	20030923	Dissection of printed edges from a fabrication layout for correcting proximity effects	716/19	716/21
11	US 6560766 B2	20030506	Method and apparatus for analyzing a layout using an instance-based representation	716/19	716/11; 716/17; 716/21; 716/4; 716/5; 716/8
12	US 6539521 B1	20030325	Dissection of corners in a fabrication layout for correcting proximity effects	716/4	716/19; 716/21
13	US 6453457 B1	20020917	Selection of evaluation point locations based on proximity effects model amplitudes for correcting proximity effects in a fabrication layout	716/19	430/5; 716/20
14	US 5923566 A	19990713	Phase shifted design verification routine	716/21	430/311; 430/322; 430/5



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1 An automated system for LSI fine pattern inspection based on comparison of SEM images and CAD data
Ito, M.;

Robotics and Automation, 1995. Proceedings., 1995 IEEE International Conference, Volume: 1 , 21-27 May 1995

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[\[Abstract\]](#) [\[PDF Full-Text \(504 KB\)\]](#) **IEEE CNF**

2 HARP: FORTRAN to silicon [compilation system]
Tanaka, T.; Kobayashi, T.; Karatsu, O.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 8 , Issue: 6 , June 1989

Pages:649 - 660

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3 The Outline Procedure in Pattern Data Preparation for Vector-Scan Electron-Beam Lithography
Komatsu, K.; Suzuki, M.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 6 , Issue: 1 , January 1987

Pages:145 - 151

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4 An ichnographic two-dimensional analysis of the MOS LSI mask layout pattern
Natori, K.;

Solid-State Circuits, IEEE Journal of , Volume: 21 , Issue: 3 , Jun 1986

Pages:457 - 463

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5 New approach to resolution limit and advanced image formation techniques in optical lithography

Fukuda, H.; Imai, A.; Terasawa, T.; Okazaki, S.;
Electron Devices, IEEE Transactions on , Volume: 38 , Issue: 1 , Jan. 1991
Pages:67 - 75

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6 An effective fault simulation method for core based LSI

Yoshida, T.; Shimoda, R.; Mizokawa, T.; Hirayama, K.;
Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian , 17-19 Nov. 1997
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7 Studies on defect inspectivity and printability by using programmed defect X-ray mask

Watanabe, H.; Kikuchi, Y.; Marumoto, K.; Matsui, Y.; Yabe, H.; Aya, S.; Okada, Takeuchi, N.;
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Microprocesses and Nanotechnology '99. 1999 International , 6-8 July 1999
Pages:12 - 13

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8 Subhalf-micron gate GaAs MESFET process using phase-shifting-mask technology

Kimura, T.; Saito, T.; Jinbo, H.; Ichioka, T.; Inokuchi, K.; Yamashita, Y.; Sandhu, S.;
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1991. Technical Digest , 1991., 13th Annual , 20-23 Oct. 1991
Pages:281 - 284

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9 Feature Size Limit of Lift-off Metallization Technology

Homma, Y.; Yajima, A.; Harada, S.;
Solid-State Circuits, IEEE Journal of , Volume: 17 , Issue: 2 , Apr 1982
Pages:142 - 147

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10 A means of reducing custom LSI interconnection requirements

Calhoun, D.F.; McNamee, L.P.;
Solid-State Circuits, IEEE Journal of , Volume: 7 , Issue: 5 , Oct 1972
Pages:395 - 404

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11 Fabrication and characteristics of NbN-based Josephson junctions 1

logic LSI circuits

Yano, S.; Tarutani, Y.; Mori, H.; Yamada, H.; Hirano, M.; Kawabe, U.;
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Pages:1472 - 1475

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12 Inspection of critical dimension- and transmission uniformity of contact patterns by DUV imaging and regression algorithm

Yamashita, K.; Yamaguchi, S.;
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13 EYESEE: A machine vision system for inspection of integrated circuit chips

Baird, M.;
Robotics and Automation. Proceedings. 1985 IEEE International Conference on , Volume: 2 , Mar 1985
Pages:444 - 448

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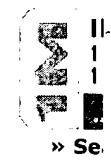
14 A new inspection method for PSM on DUV inspection light source

Isomura, I.; Tsuchiya, H.; Sugihara, S.; Yamashita, K.; Tabata, M.;
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Pages:64 - 65

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1 High accurate optical proximity correction under the influences of aberration in 0.15 μm logic process

Harazaki, K.; Hasegawa, Y.; Shichijo, Y.; Tabuchi, H.; Fujii, K.;
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Applied Superconductivity, IEEE Transactions on , Volume: 11 , Issue: 1 , Mar
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3 Hierarchical optical proximity correction on contact hole layers

Yamamoto, K.; Kobayashi, S.; Uno, T.; Kotani, T.; Tanaka, S.; Inoue, S.;
Watanabe, S.; Higurashi, H.;

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4 A 5-μm² full-CMOS cell for high-speed SRAMs utilizing a optical-proximity-effect correction (OPC) technology

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VLSI Technology, 1996. Digest of Technical Papers. 1996 Symposium on , 11-June 1996
Pages:146 - 147

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5 A cost-driven lithographic correction methodology based on off-the-sizing tools

Gupta, P.; Kahng, A.B.; Sylvester, D.; Yang, J.;
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Numerical Modeling of Processes and Devices for Integrated Circuits, 1994. NI V., International Workshop on , 5-6 June 1994
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8 Practical applications of 2-D optical proximity corrections for enhanced performance of 0.25 μm random logic devices

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Schellenberg, F.;
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11 An object-based approach to optical proximity correction

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13 Low energy e-beam proximity lithography (LEEPL)

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15 Layout design methodologies for sub-wavelength manufacturing

Rieger, M.L.; Mayhew, J.P.; Panchapakesan, S.;
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16 A statistical gate CD control including OPC

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17 Application of full chip OPC to quarter micron logic device

Kyune-Jin Shim; Ki-Yeop Park; Won Gyu Lee; Dai-Hoon Lee;
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18 Advanced gate etching for accurate CD control for 130-nm node AS manufacturing

Nagase, M.; Tokashiki, K.;

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Pages:281 - 285

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20 248nm lithography of 2D photonic crystal waveguide with optical proximity correction

Teo, H.G.; Yu, M.B.; Doan, M.T.; Singh, J.; Sun, H.Q.; Liu, A.Q.;

Biophotonics/Optical Interconnects and VLSI Photonics/WBM Microcavities, 2004 Digest of the LEOS Summer Topical Meetings , 28-30 June 2004

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Nasuno, T.; Matsubara, Y.; Minami, A.; Uchida, N.; Kobayashi, H.; Aoyama, H. Tsuda, H.; Tsujita, K.; Wakamiya, W.; Kobayashi, N.;

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